REMARKS

In response to the Office Action dated February 4, 2009 Applicant respectfully requests reconsideration based on the above claim amendments and the following remarks. Applicant respectfully submits that the claims as presented are in condition for allowance.

Claims 1-16 are pending in the present Application. Claims 1, 7 and 14 are amended, and Claims 12 and 13 are cancelled, leaving Claims 1-11 and 14-17 for consideration upon entry of the present amendments and the following remarks.

Support for the claim amendments is at least found in the specification, the figures, and the claims as originally filed. Particularly, support for amended Claims 1, 7 and 14 is at least found in originally filed Figure 4, and in the specification at page 7, lines 14-24, page 8, line 24 to page 9, line 4 and page 13, lines 12-23. Claim 14 is amended to provide proper dependency due to the cancellation of Claims 12 and 13.

No new matter has been introduced by these amendments. Reconsideration and allowance of the claims are respectfully requested in view of the above amendments and the following remarks.

Claim Rejections under 35 U.S.C. §103

Claims **1**-17 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Kawaguchi et al., U.S. Patent No. 5,592,199 (hereinafter "Kawaguchi"), in view of Kubota et al., U.S. Patent No. 6,791,526 (hereinafter "Kubota"), and further in view of Nakamura et al., U.S. Patent No. 7,136,058 (hereinafter "Nakamura"). Applicant respectfully traverses the rejections for the reasons set forth below.

Claims 12 and 13 are hereinabove cancelled and rejections are rendered moot for these claims. Claim 14 is amended to depend from independent Claim 1 due the cancellation of Claims 12 and 13.

Amended independent **Claims 1 and 7** similarly recite, *inter alia*:

"an LCD panel displaying images and including:
a first substrate;
a second substrate facing the first substrate, a plurality of pixels being provided on the second substrate;
a common electrode disposed on the first substrate;
gate lines disposed on the second substrate and opposing the common electrode, the gate lines receiving a gate driving signal;

data lines for supplying image data signals to the pixels; and

an output instruction signal line disposed on the second substrate and opposing the common electrode;

a data driver disposed on a data tape carrier package (TCP);

a gate driver outputting a gate driving signal to the LCD panel; and

a timing controller providing a first control signal to the gate driver so as to control an output of the gate driving signal, and providing an output instruction signal to the data driver via the output instruction signal line *to delay the output instruction signal depending on a capacitive load and a resistive load formed by the output instruction signal line and the common electrode*,

wherein *the data driver outputs a delayed image data signal to the LCD panel as the output instructions signal is delayed*."

Regarding Kawaguchi in the instant Office action at Pages 3, 4, 8 and 9, peripheral portion 227 of substrate 222, common lines 231, flexible wiring boards 230 along y-axis with six drive IC's 229, and connector 8/control board 232 (Figure 1, Col. 19, lines 15-18/Figure 30, Col. 28, lines 6-14) in Figures 30-32 of Kawaguchi are respectively considered as teaching the "second substrate," the "output instruction signal line," the "data TCP," and the "timing controller" of independent Claims 1 and 7.

It is conceded on Pages 4 and 9 of the instant Office action that Kawaguchi does not disclose that the timing of the output of image data is according to a delay of the gate driving signal. Applicant respectfully submits that Nakamura also does not disclose that the timing of the output of image data is according to a delay of the gate driving signal.

Regarding Kubota in the instant Office action with respect to independent Claims 1 and 7 at Pages 4 and 9, Figure 18 of Kubota is relied upon as allegedly teaching that a timing of an output of image data is according to a delay of a gate driving signal.

In amended independent Claims 1 and 7, "the output instruction signal is delayed *depending on a capacitive load and a resistive load formed by the output instruction signal line and the common electrode*." Furthermore, amended independent Claims 1 and 7 include "*the data driver outputs a delayed image data signal to the LCD panel as the output instructions signal is delayed.*"

Figure 18 of Kubota is a diagram depicting the timing of shift data and gate line driving signals in the TFT gate drive circuit shown in Figure 15 which illustrates an example of a conventional TFT gate drive circuit with three voltage levels. Applicant respectfully submits

that Kubota *does not teach or suggest* **an output instruction signal is delayed** depending on a capacitive load and a resistive load formed by the output instruction signal line and the common electrode, and **a data driver outputs a delayed image data signal** to the LCD panel as the output instructions signal is delayed of amended independent Claims 1 and 7, and does not remedy the deficiencies of Kawaguchi and Nakamura.

It is further conceded on Pages 4 and 9 of the instant Office action that Kawaguchi and Kubota do not disclose a common electrode disposed on the first substrate or that the output instruction signal line opposes the common electrode of independent Claims 1 and 7.

Regarding Nakamura in the instant Office action with respect to independent Claims 1 and 7 at Pages 5, 9 and 10, Nakamura is relied upon as allegedly teaching a common electrode disposed on the first substrate and opposing signal line. At Pages 5 and 10 of the instant Office action, Col. 4, lines 10-19, power supply wiring pattern P1 and capacitor elements C4,C5 wiring in Figures 14 and 15 of Nakamura are relied upon as teaching "signal lines" disposed on the second substrate and opposing the common electrode.

Nakamura teaches signal lines through which an amplified and D/A converted analog *video signal* passes. (See, for example, Col. 4, lines 10-11 and 21-24.) Nakamura teaches *power supply wiring* pattern P1 of AMP 17 which amplifies an output from the DAC 16, overlaps common electrode 23. (See, Col. 15, lines 43-48.) Nakamura further teaches capacitor elements C4 and C5 are connected between stages of inverters IV1 to IV 3 *in the AMP 17.* (See, Col. 15, lines 51-55 and Figure 15.) That is, the lines through which an amplified and D/A converted analog *video signal* passes, the *power supply* wiring P1 and the wiring of capacitor elements C4 and C5 within AMP 17 in Nakamura, does not provide "an output instruction signal" as claimed, which is not a data signal. Therefore, Nakamura *does not teach or suggest* an **output instruction** signal line disposed on the second substrate and opposing the common electrode, **the output instruction signal being delayed** depending on a capacitive load and a resistive load formed by the **output instruction** signal line and the common electrode, and **a data driver outputs a delayed image data signal** to the LCD panel **as the output instructions signal** is delayed of amended independent Claims 1 and 7, and does not remedy the deficiencies of Kawaguchi and Kubota.

Thus, Kawaguchi, Kubota and Nakamura, alone or in combination, *fail to teach or suggest all of the limitations* of similarly amended independent Claims 1 and 7. Accordingly, *prima facie* obviousness does not exist regarding amended Claims 1 and 7 with respect to Kawaguchi, Kubota and Nakamura. Applicant respectfully submits that Claims 1 and 7, and Claims 2-6, 8-11 and 14-17 as respectively depending from Claims 1 and 7, are not further rejected or objected, and are therefore allowable. Entry of the claim amendments, reconsideration, withdrawal of the relevant §103 rejections and allowance of Claims 1-11 and 14-17 are respectfully requested.

Conclusion

All of the objections and rejections are herein overcome. In view of the foregoing, it is respectfully submitted that the instant application is in condition for allowance. No new matter is added by way of the present Amendments and Remarks, as support is found throughout the original filed specification, claims and drawings. Prompt issuance of Notice of Allowance is respectfully requested.

The Examiner is invited to contact Applicant's attorney at the below listed phone number regarding this response or otherwise concerning the present application.

Applicant hereby petitions for any necessary extension of time required under 37 C.F.R. 1.136(a) or 1.136(b) which may be required for entry and consideration of the present Reply.

If there are any charges due with respect to this Amendment or otherwise, please charge them to Deposit Account No. 06-1130 maintained by Applicant's attorneys.

Respectfully submitted,

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